Course No: SWEN 2301
Course Title: Electronics Principles
Date: 11/01/2018
No. of Questions: (3)
Time: 2 hours
Using Calculator (No)

University of Palestine

Final Exam
1st. 2018-2017
Total Grade: 50

Instructor Name: Eng. M. Timraz
Student No.: _____
Student Name: _____
College Name: _____
Dep. / Specialist: _____
Using Dictionary (No)

Question One: (10/50)

Chose the correct answer, then put it in the following table

1	2	3	4	5	6	7	8	9	10

1. Three different Q points are shown on a dc load line. The upper Q point represents the:
   a) minimum current gain
   b) intermediate current gain
   c) maximum current gain
   d) cutoff point
2. A transistor has a β_{DC} of 250 and a base current, IB, of 20 μ A. The collector current, IC, equals:
   a) 500 µ A
   b) 5 mA
   c) 50 mA
   d) 5 A
3. When transistors are used in digital circuits they usually operate in the:
   a) active region
   b) breakdown region
   c) saturation and cutoff regions
   d) linear region
4. Voltage-divider bias provides:
   a) an unstable Q point
   b) a stable Q point
   c) a Q point that easily varies with changes in the transistor's current gain
   d) a Q point that is stable and easily varies with changes in the transistor's current gain
5. A current ratio of IC/IE is usually less than one and is called:
   a) beta
   b) theta
   c) alpha
   d) omega

6. With the positive probe on an NPN base, an ohmmeter reading between the other transistor terminals should be:
   a) open
   b) infinite
   c) low resistance
   d) high resistance
7. In a Common-Emitter configuration, an emitter resistor is used for:
   a) stabilization
   b) ac signal bypass
   c) collector bias
   d) higher gain
8. To operate properly, a transistor's base-emitter junction must be forward biased with reverse bias applied to which junction?
   a) collector-emitter
   b) base-collector
   c) base-emitter
   d) collector-base
9. The ends of a load line drawn on a family of curves determine:
   a) saturation and cutoff
   b) the operating point
   c) the power curve
   d) the amplification factor
10. What is the current gain for a common-base configuration where IE = 4.2 mA and IC = 4.0 mA?
   a) 16.80
   b) 1.05
   c) 0.20
   d) 0.95

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Question Two: (10/50)

Which of the following statements is true or false?
Please put √or × below the question's number in the following table

1	2	3	4	5	6	7	8	9	10

1. A decrease in base current of a C-E amplifier causes the voltage measured between the emitter and the collector to increase.
2. The voltage measured from the collector to the emitter is the sum of the voltage base-emitter plus the voltage collector-base.
3. This is a PNP transistor. 
4. A transistor used in a digital circuit will have two operating states, which are cutoff and saturation.
5. In a BJT, the collector current is approximately equal to the base current.
6. The voltage gain of a transistor is inversely proportional to the change in output current.
7. When troubleshooting a bipolar junction transistor using an ohmmeter, if one of the junctions reads low in both directions, the junction is shorted and the transistor is bad. If one of the junctions reads high in both directions, the junction is shorted and the transistor is good.
8. A common-emitter (C-E) is so called because the emitter is connected to both the input and output signals.
9. With a common-collector (C-C) amplifier the input is applied to the base and the output is taken from the emitter.
10. V_{CE} approximately equals Vcc when a transistor switch is cut off.

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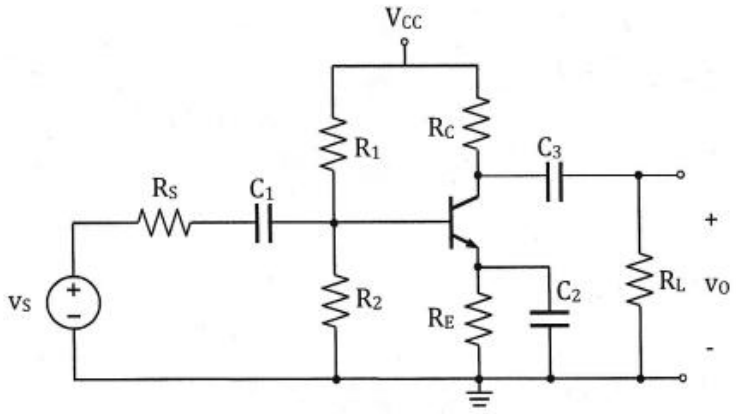
Question Three: (10/50)

A) Consider the common emitter amplifier given in the following circuit; ***5 Pt.***

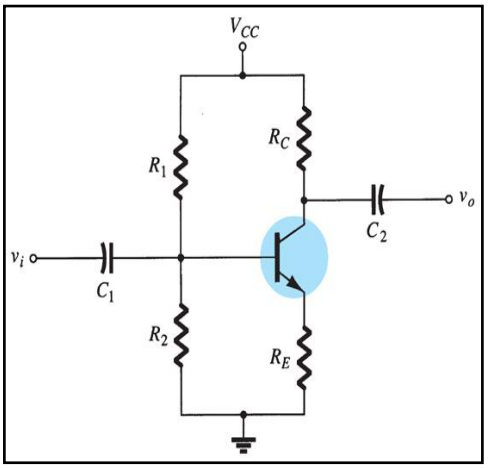


Circuit Parameters
$V_{CC} = 12$ V
$R_1 = 100$ K
$R_2 = 15$ K
$R_E = 1$ K
$R_C = 4$ K
$R_S = 1$K
$R_L = 12$ K

Transistor Parameters
$\beta = 100$
$V_{BE(ON)} = 0.7$ V
$V_A = \infty$

Under DC conditions, determine the voltage gain.

B) If V_{CC} = +18 V, voltage, R1 is 4.7 k Ω, and R2 is 1500Ω. ***5 Pt.***
What is the base bias voltage?
What are the collector and emitter currents?



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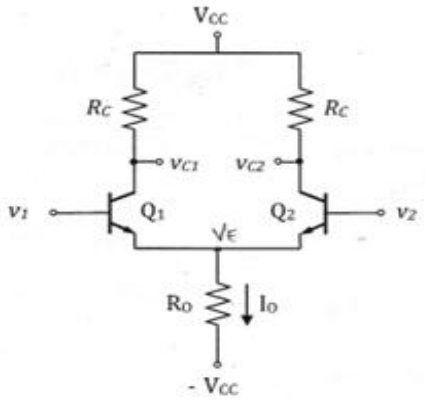
Question Four: (05/50)

A) Determine Ro to set $I_{c1} = I_{c2} = 2mA$? ***5 Pt.***

Let $V_1 = V_2 = 0$ in the DC analysis.

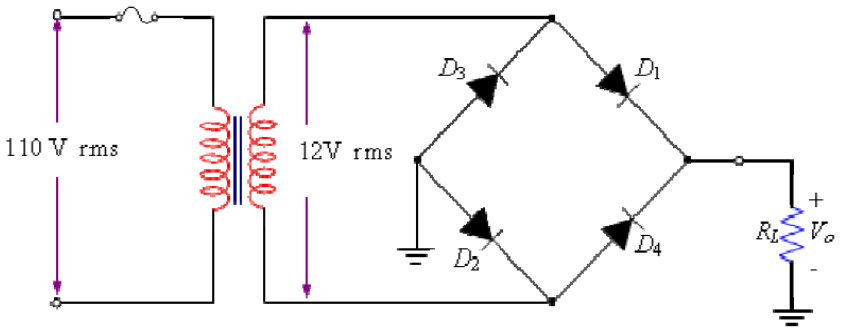
Where $I_E = I_{E1} + I_{E2}$



Circuit Parameters
$V_{CC} = 12$ V
$R_C = 3$ kΩ

Transistors' Parameters
$V_{T1} = 27$ mV
$V_{T2} = 25$ mV
$\beta = 100$
$V_{BE(on)} = 0.7$ V
$V_A = \infty$

B) Determine the maximum voltage for the output shown circuit and PIV for each Si diode? ***5 Pt.***



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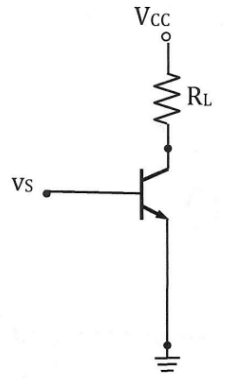
Question Five: (05/50)

A) For the following amplifier circuit: ***2.5 Pt.***

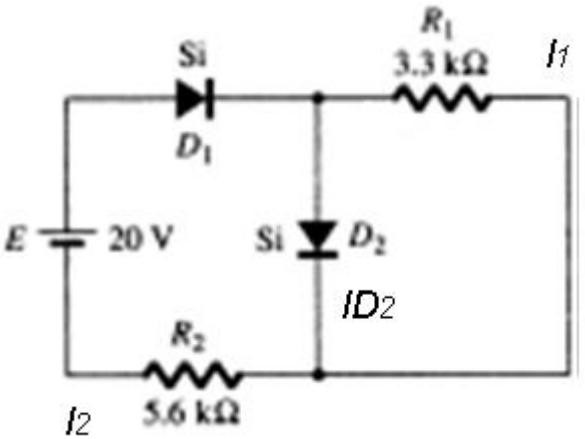
a) Draw the DC load line and determine the class of power amplifier.

b) Determine I_{CQ} assuming the Q point is at the center of the DC load line.

Where V_{CC} = 15 V, R_L = 15 and $V_{CE(SAT)}$ = 0V.



B) Determine the currents I_1, I_2, and I_{D2} for the network of the following figure. Where R_1=3.3 kΩ, R_2=5.6 kΩ. ***2.5 Pt.***



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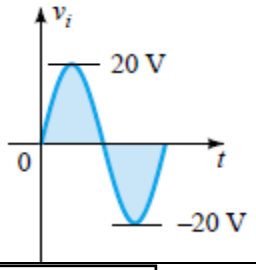
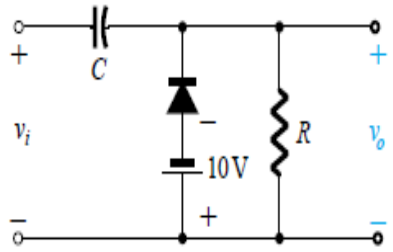
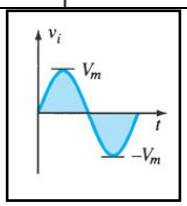
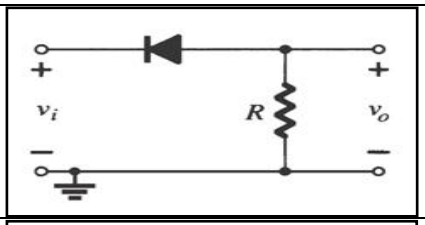
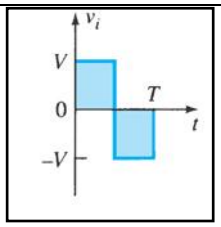
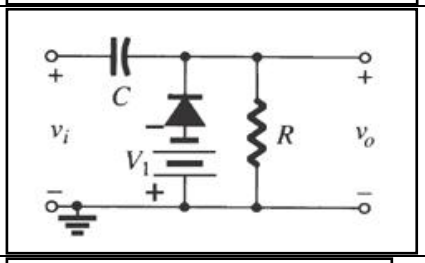
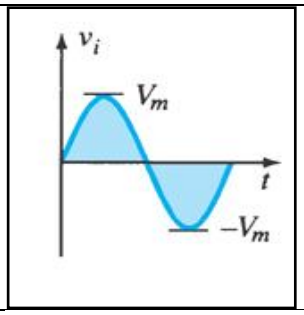
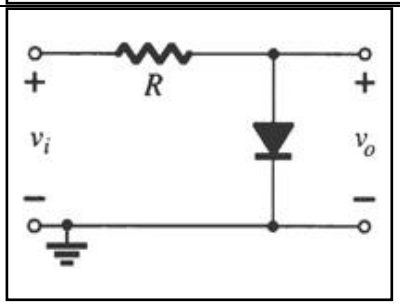
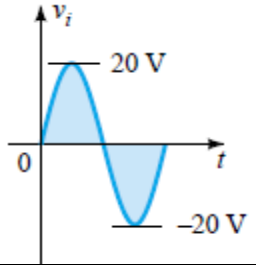
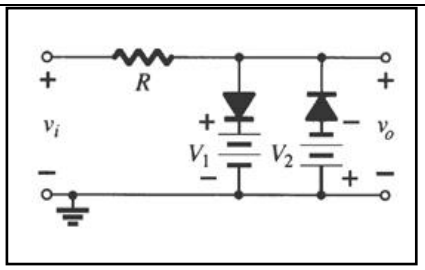
Question Six: (5/50)

Draw the output signal for each figure below.

No.	Input	Circuit	Output
1.			
			
			
4.			
5.			

End of Questions
Good Luck